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EXAMINER	
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ART UNIT	PAPER NUMBER
2128	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/774,990	AMATANGELO ET AL.	
	Examiner	Art Unit	
	SHAMBHAVI PATEL	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6,8-10 and 16-20* is/are pending in the application.

4a) Of the above claim(s) *6,8-10 and 16-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-4 have been presented for examination.

Response to Arguments

3. In view of Applicant's arguments and the evidence presented in Weste et al., the 35 U.S.C. 112 2nd rejection of the terms "evaluate node", "dynamic circuit", "labeling" and "dynamic signal" are withdrawn.

4. In view of Applicant's amendments, the 35 U.S.C. 112 2nd rejection regarding the omission of essential steps is withdrawn.

5. In view of Applicant's amendments, the 35 U.S.C. 101 rejection is withdrawn.

6. Applicant's arguments with respect to the 35 U.S.C. 102 and 35 U.S.C. 112 rejection of claims 1-4 have been fully considered but are not persuasive.

Regarding the 35 U.S.C. 112 rejection:

i. **Applicant submits,** on page 6 of the remarks, that the term "near dynamic circuit" is not "insolubly ambiguous" in light of the specification.

Examiner notes that Applicant has not provided sufficient evidence to overcome the 35 U.S.C. 112 rejection of the term "near dynamic circuit". While Applicant has provided evidence suggesting that it is well-known in the art that a domino circuit is a species of a dynamic circuit genus, no evidence has been provided to support Applicant's claim that a "near dynamic circuit" is a genus of the species "near domino circuit". Thus, the definitions of the terms "near domino circuit" and "near domino gate" provided in the specification are of no relevance to the term "near dynamic circuit". Applicant submits (emphasis added) "…the claim term 'near dynamic circuit' ***may refer, in some embodiments,*** to a combinatorial logic gate whose inputs receive a data signal and a clock signal and whose output provides a data signal that is dynamic in nature." Examiner notes that this is not a definitive definition of the term "near dynamic circuit"—it is merely a definition that **may possibly** be used in **some** of the embodiments. The specification does not provide a definition of the term "near dynamic circuit", nor has Applicant provided any evidence that the term has a specific and well-known definition in the art. The rejection is maintained.

Regarding the prior art rejection:

ii. **Applicant submits,** on page 7 of the remarks, "During the Examiner interviews, Examiner Patel indicated that she would withdraw the 102 rejections for claims 1, 3 and 4 because *Norton* only labels notes as either clock, data, dynamic, latch or gated, and does not label them as 'near dynamic', which is illustrated in Fig. 3 and described in paragraphs 29."

Examiner notes that the withdrawal of the rejection was contingent on Applicant's providing evidence that the term "near dynamic circuit" has a specific and well-known definition in the art and/or providing support from the specification that defines the term. Applicant states that paragraph 0029 of the specification defines the term "near dynamic circuit". However, Examiner notes that the cited portion of the specification (provided below) does not define the term:

> Referring to FIG. 2, a flow chart of a method for determining how to model a combinatorial gate is shown. The combinatorial block determinator module 140 determines whether to model a combinatorial logic block as a clock gate or as a near domino gate. A clock gate model receives a data signal and a clock signal as inputs and provides a clock signal output. A near domino gate receives a data signal and a clock signal as inputs and provides a data signal as an output.

The specification does not provide a definition of the term "near dynamic circuit", nor has Applicant provided any evidence that the term has a specific and well-known definition in the art. Applicants have not provided sufficient evidence that the claims are distinguishable from the prior art, and the rejections is maintained.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. **Claims 1-4 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite** for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Regarding **claim 1**, the term "near dynamic circuit" is vague and indefinite. All other claims are rejected by virtue of their dependency.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1, 3 and 4 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by **Norton ("Transistor-level Sizing and Timing Verification of Domino Circuits in the Power PC Microprocessor"** 1997**).**

Regarding claim 1:

Norton discloses a computer-implemented method of modeling the static timing behavior of a combinatorial gate comprising:

a. determining that a data signal has been propagated to a first input of the combinatorial gate **(section 4.1 1st-2nd paragraphs: footed and footless gates have both data and clock signal inputs)**

b. determining that a clock signal has been propagated to a second input of the combinatorial gate **(section 4.1 1st-2nd paragraphs: footed and footless gates have both data and clock signal inputs)**

c. determining that an output signal of the combinatorial gate has been propagated to an evaluate node of a dynamic circuit **(section 4.3 1st paragraph: output is an input to another domino circuit)**

d. labeling the combinatorial gate as a near dynamic circuit **(section 4.2: classified as dynamic nodes)**

e. modeling the output signal of the combinatorial gate as a dynamic signal **(figure 2; section 4.3 1st paragraph)**

f. storing the modeled output signal in a report **(figures 5 and 6: waveforms).**

Regarding claim 3:

Wang discloses the method of claim 1 propagating the data signal includes includes causing a later arriving edge of the data signal to cause the output signal to respond **(section 4.3)**

Regarding claim 4:

Wang discloses the method of claim 1 wherein: the data signal includes a single edge per clock period; and, when propagating the data signal, the single edge is propagated through the combinatorial gate **(figure 2; section 4.3).**

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

9. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Norton ("Transistor-level Sizing and Timing Verification of Domino Circuits in the Power PC Microprocessor"** 1997) **in view of Zhao ("Timing-Driven Partitioning and Timing Optimization of Mixed Static-Domino Implementations",** 2000).

Regarding claim 2:

Norton does not explicitly disclose the method of claim 1 further comprising performing a reverse traversal function on a circuit design containing the combinatorial gate. **Zhao teaches** performing reverse traversals on circuit designs containing both static and domino circuits **(Zhao: page 1329 "Determining the Candidate Cut Nodes" reverse PERT traversal).** At the time of the invention, it would have been obvious to one of ordinary skill in the art to combine the teachings of Norton and Zhao because the methodology of Zhao minimizes implementation costs while meeting timing constraints **(Zhao: section III page 1332 left column 2nd complete paragraph).**

Conclusion

10. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Examiner's Remarks: Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner. In the case of amending the claimed invention,

Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on for proper interpretation and also to verify and ascertain the metes and bounds of the claimed invention.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shambhavi Patel whose telephone number is (571) 272-5877. The examiner can normally be reached on Monday-Friday, 8:00 am – 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571) 272-22792279. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SKP

/Kamini S Shah/
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